

[illegible]

Abstract of Disclosure

A management system is provided for access control modes of a dynamic random access memory (DRAM) module socket. The management system includes a basic input/output system (BIOS), an integrated chipset, two switches, and a DRAM module socket. The two switches are respectively connected between an ECC/CKE and a DQM/CKE mode output port of the integrated chipset, and an ECC, a CKE, and a DQM mode input port of the DRAM module socket. The management system utilizes general purpose input/output (GPIO) terminals of the integrated chipset to control on/off states of the two switches so as to switch between both the ECC, the CKE, and the DQM mode input ports of the DRAM module socket. Software reconfigurations, by way of the BIOS, for DRAM access control modes are thus made possible.

Figures